IN THE CLAIMS

Please amend the following claims which are pending in the present application:

1. (Currently amended) A substrate of an integrated circuit package, comprising:

a base structure, including at least a portion having a low k-value, having upper and lower sides and a plurality of via openings formed therein;

a conductive via in each via opening, the conductive vias including at least power and ground vias; and

first and second capacitor structures on the upper and lower sides of the base structure respectively, each capacitor structure including conductive power and ground planes and a dielectric layer, having a high k-value, between the power and ground planes, the power and ground planes being electrically connected to at least one of the power and ground vias, respectively.

2. (Original) The substrate of claim 1, wherein the base structure is made of a sintered ceramic material.

3. (Original) The package substrate of claim 1, wherein the vias include signal vias, each signal via being electrically disconnected from both the power and ground planes.

4. (Currently amended) The substrate of claim 3, wherein ~~the dielectric layer of the capacitor structure is made of a dielectric material with a high k-value, the substrate having first and second portions, the first portion having the high k-value dielectric material and the second portion not having the high k-value dielectric material,~~ the signal vias being formed in the ~~second~~ portion have the low k-value material.

5. (Currently amended) An integrated circuit package, comprising:

a base structure, including at least a portion, having upper and lower sides and a plurality of via openings formed therein;

a conductive via in each via opening, the conductive vias including at least power and ground vias; and

first and second capacitor structures on the upper and lower sides of the base structure respectively, each capacitor structure including conductive power and ground planes and a dielectric layer, having a high k-value, between the power and ground planes, the power and ground planes being electrically connected to at least one of the power and ground vias, respectively; and

a die having an integrated circuit formed therein mounted on the substrate.

6. (Original) The integrated circuit package of claim 5, wherein the substrate is an interposer substrate, further comprising:

a package substrate, the interposer substrate being mounted to the package

substrate.

7. (Original) The integrated circuit package of claim 6, wherein the vias are connected to contacts on the package substrate without an x-y transformation.

8. (Original) The integrated circuit package of claim 5, wherein the vias include signal vias, each signal via being electrically disconnected from both the power and ground planes.

9. (Currently amended) The integrated circuit package of claim 8, wherein ~~the dielectric layer of the capacitor structure is made of a dielectric material with a high k-value, the substrate having first and second portions, the first portion having the high k-value dielectric material and the second portion not having the high k-value dielectric material,~~ the signal vias being formed in the ~~second~~ portion have the low k-value material.

10-16. (Cancelled)